

Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action in the above-identified patent application. Claims 7, 11, 24 and 25 are allowed. Claims 39 and 45 have been amended.

Claims 42-43 and 46-47 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 39-43 and 45-47 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 38 and 40-47 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.* (U.S. Patent No. 6,556,088).

Claims 38 and 39 are rejected under 35 U.S.C. §102(b) as being anticipated by *Maneatis* (U.S. Patent No. 5,727,037).

I. Rejection of Claims 42-43 and 46-47 under 35 U.S.C. §112, First Paragraph

Claims 42-43 and 46-47 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

In rejecting claims 42-43 and 46-47, the Examiner stated: “There is no description for the limitations ‘a phase mixer’ and ‘a clock buffer’ as recited in these claims. Further, drawings do not show these limitations.” Office Action, page 2.

The Applicant’s attorney respectfully disagrees. A description of “a phase mixer” and “a clock buffer” is at least at page 3, lines 14-17 of the instant Application. In particular, the instant Application identifies “a phase mixer” and “a clock buffer” as “circuit components of the PLL/DLL [102,103, 112, 113]” shown in Figs. 1a-b.

It is therefore respectfully requested that the rejection of claims 42-43 and 46-47 under 35 U.S.C. §112, first paragraph, be withdrawn.

II. Rejection of Claims 39-43 and 45-47 under 35 U.S.C. §112, Second Paragraph

Claims 39-43 and 45-47 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 39 and 45 have been amended so that “the charge-pump includes a semiconductor device to provide the first bias current...”

In rejecting claims 40-43, the Examiner stated:

[T]he limitations “a second”, “a third,” “a fourth bias” and “a fifth” current(s) recited in these claims also appear to be misdescriptive since drawings disclose a single bias current I_d outputted from “the voltage regulator.” Office Action, page 3.

The Applicant’s attorney respectfully disagrees and respectfully directs the Examiner to at least pages 5-6, lines 27-29 and 1-6 as well as page 3, lines 14-17 and pages 11-12, lines 18-29 and 1-6 of the instant Application.

In rejecting claims 42 and 43, the Examiner stated:

[T]he limitation “phase mixer” of claim 42 appears to referring to “voltage controlled oscillator” as recited in claim 38 since there is no component in drawings would be best fitted to be considered “phase mixer.” Lastly, the limitation “clock buffer” of claim 43 appears referring to one of components recited earlier since there is no other component in figures meet the limitation “clock buffer.” Office Action, page 3.

The Applicant’s attorney respectfully disagrees. A description of “a phase mixer” and “a clock buffer” is at page 3, lines 14-17 of the instant Application. In particular, the instant Application identifies “a phase mixer” and “a clock buffer” as “circuit components of the PLL/DLL [102,103, 112, 113]” shown in Figs. 1a-b.

It is therefore respectfully requested that the rejection of claims 39-43 and 45-47 under 35 U.S.C. §112, second paragraph, be withdrawn.

III. Rejection of Claims 38 and 40-47 under 35 U.S.C. §102(e)

Claims 38 and 40-47 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dietl et al.*

Claim 38 calls for “wherein the voltage regulator provides a first bias current to the charge-pump based on the load current.” This limitation has not been identified by the Examiner as being disclosed in *Dietl et al.* The Examiner states that “a load current” is provided by voltage V_{PN} on the trace from voltage regulator 95 to charge pump 91 (Office Action, page 4), but has not identified where *Dietl et al.* discloses “a first bias current.”

Claims 40-43 depend from claim 38 and therefore are patentable for at least the reasons stated above.

Further, the Examiner has not identified where *Dietl et al.* discloses “a phase mixer” and “clock buffer” as called for in claim 42 and 43.

In rejecting claim 44, the Examiner stated:

It is noted that pre-ample [sic, preamble] is not given patentable weight. Besides, a delay locked loop circuit (DLL) and phase locked loop circuit are seen as equivalent circuits in the art. Office Action, page 5.

The Applicant's attorney respectfully disagrees. Under a proper 35 U.S.C. §102(e) rejection, the Examiner must identify each claimed element in a single cited reference. Claim 44 calls for "a voltage controlled delay line" that the Examiner has not identified as being disclosed in *Dietl et al.*

Claims 45-47 depend from claim 44 and therefore are patentable for the reasons stated above in regard to claim 44.

Further, the Examiner has not identified in *Dietl et al.* "a semiconductor device to provide the first bias current..." as called for in claim 45.

Further, the Examiner has not identified in *Dietl et al.* "a phase mixer..." and "a clock buffer..." as required by claims 46 and 47.

It is therefore respectfully requested that the rejection of claims 38 and 40-47 under 35 U.S.C. §102(e) be withdrawn.

IV. Rejection of Claims 38 and 39 under 35 U.S.C. §102(b)

Claims 38 and 39 are rejected under 35 U.S.C. §102(b) as being anticipated by *Maneatis*.

Claim 38 calls for "wherein the voltage regulator provides a first bias current to the charge-pump based on the load current." This limitation has not been identified by the Examiner as being disclosed in *Maneatis*. The Examiner states that "a load current" is provided by voltage V_{PN} on line 134 from "a voltage regulator 110" and contradictorily states the distinctly claimed "a first bias current" is the same current: "(i.e. current on trace from bias generator 110 to charge pump 105)..." Office Action, page 5.

In regard to claim 39, the Examiner has not identified with particularity which "transistor" in Fig. 2 of *Maneatis* discloses the claimed "a semiconductor device to provide the first bias current in response to the load current."

It is therefore respectfully requested that the rejection of claims 38 and 39 under 35 U.S.C. §102(b) be withdrawn.

Based on the above amendments and these remarks, reconsideration of the presently pending claims is respectfully requested.

Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: November 28, 2006

By: /Kirk J. DeNiro/
Kirk J. DeNiro
Reg. No. 35,854

VIERRA MAGEN MARCUS & DENIRO LLP
575 Market Street, Suite 2500
San Francisco, California 94105
Telephone: (415) 369-9660
Facsimile: (415) 369-9665